FPGA-BASED AUTOMATIC WASHING MACHINE CONTROL SYSTEM USING VERILOG HDL

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ABSTRACT

Automatic washing machines have become an essential household appliance because they simplify the clothes washing process, reduce manual effort, minimize water consumption, and improve washing efficiency. Conventional washing machines generally use microcontroller-based controllers or electromechanical timers to manage washing operations such as water filling, washing, rinsing, and spinning. However, these traditional controllers often experience limited processing speed, reduced flexibility, increased maintenance complexity, and slower response during sequential control operations. Recent advancements in Digital System Design, Field Programmable Gate Arrays (FPGA), Verilog Hardware Description Language (HDL), and Finite State Machine (FSM) architectures have enabled the development of high-speed hardware controllers capable of performing automatic washing operations with greater reliability and deterministic execution. This project presents the Design of an Automatic Washing Control System Using Verilog HDL. The proposed controller is implemented using Verilog HDL on an FPGA platform, integrating a water level sensing module, door lock controller, wash cycle controller, rinse controller, spin controller, timer module, motor control unit, LCD display interface, and Finite State Machine (FSM) into a unified hardware architecture. Initially, the controller receives the selected washing mode and continuously monitors the water level and door status before initiating the washing process. The FSM sequentially controls water filling, detergent mixing, washing, rinsing, spinning, and cycle completion while ensuring safe operation throughout the washing cycle. The system continuously supervises water level, motor operation, and timer status to maintain reliable washing performance. Experimental evaluation demonstrates high washing cycle accuracy, reliable state transitions, low processing delay, efficient FPGA resource utilization, and stable hardware operation under different washing conditions. The proposed FPGA-based controller significantly improves washing automation, reduces controller complexity, minimizes execution time, enhances operational reliability, and provides a scalable and cost-effective solution for next-generation intelligent washing machine control systems.

Keywords: Verilog HDL, FPGA, Automatic Washing Machine, Finite State Machine (FSM), Digital Controller, Embedded Systems, Hardware Description Language, Washing Control System, Motor Control, Digital Logic.

I. INTRODUCTION

Automatic washing machines have become indispensable household appliances because they simplify the clothes washing process, reduce manual effort, improve cleaning efficiency, and save both water and electrical energy. Modern washing machines perform multiple sequential operations including water filling, detergent mixing, washing, rinsing, draining, and spinning through automated control mechanisms. Conventional washing machines generally employ electromechanical timers or microcontroller-based controllers to manage these operations. However, these traditional control systems often suffer from limited processing capability, slower response, increased hardware complexity, reduced flexibility, and higher maintenance requirements. Mechanical timer failures and software execution delays may further reduce the overall reliability of washing operations. Therefore, there is an increasing demand for high-speed digital controllers capable of performing sequential washing operations with deterministic execution and improved reliability. Recent advancements in Digital System Design, Field Programmable Gate Arrays (FPGA), Verilog Hardware Description Language (HDL), Finite State Machine (FSM) architecture, and embedded hardware systems have enabled the development of intelligent washing machine controllers with faster processing speed, lower power consumption, and greater operational stability. FPGA-based controllers execute washing operations directly in hardware, significantly improving response time, resource utilization, and system reliability for modern smart home appliances [1–8].

Modern automatic washing machines integrate multiple sensors, actuators, digital controllers, and embedded processing units to automate the complete washing cycle. Water level sensors continuously monitor the quantity of water inside the washing drum, while door lock sensors ensure user safety before motor operation begins. Motor controllers regulate drum rotation during washing, rinsing, and spinning stages according to predefined timing sequences. Finite State Machine (FSM)-based digital controllers have become increasingly popular because they efficiently manage sequential washing operations through predefined hardware states such as Idle, Water Fill, Wash,

Drain, Rinse, Spin, and Completion. Verilog HDL enables designers to implement these digital controllers directly on FPGA devices, providing deterministic timing, modular hardware design, and simplified system verification. Experimental investigations demonstrate that FPGA-based washing controllers offer higher processing speed, improved reliability, efficient hardware utilization, lower execution delay, and enhanced operational safety compared with conventional software-based controllers [9–17].

This project proposes the Design of an Automatic Washing Control System Using Verilog HDL to provide a reliable, high-speed, and hardware-efficient washing machine controller for modern domestic appliances. The proposed framework implements the controller using Verilog HDL on an FPGA platform, integrating a water level sensing module, door lock controller, wash cycle controller, rinse controller, spin controller, timer module, motor control unit, LCD display interface, and Finite State Machine (FSM) into a unified hardware architecture. Initially, the controller continuously receives the selected washing mode and verifies both the door lock status and water level before initiating the washing cycle. The FSM sequentially controls water filling, detergent mixing, washing, draining, rinsing, spinning, and cycle completion according to predefined timing parameters. Throughout system operation, the controller continuously supervises sensor inputs, motor activity, and timer values to ensure safe and reliable washing performance. The effectiveness of the proposed controller is evaluated using engineering parameters including washing cycle accuracy, timer accuracy, motor control efficiency, water level detection accuracy, processing speed, hardware resource utilization, response time, and overall system reliability. Experimental evaluation demonstrates that the FPGA-based washing controller accurately executes washing sequences, efficiently utilizes hardware resources, minimizes processing delay, and provides stable operation, making it suitable for next-generation intelligent washing machine control systems [18–25].

II. SURVEY OF RESEARCH

1. Automatic Washing Machine Control Systems

Automatic washing machine control systems have become an important application of embedded electronics and digital automation because they simplify household operations and improve washing efficiency. Researchers have developed intelligent washing controllers capable of automatically performing water filling, washing, rinsing, draining, spinning, and cycle completion with minimal human intervention. Conventional washing machines generally employ electromechanical timers or microcontroller-based controllers that perform sequential operations based on predefined timing schedules. However, these controllers often experience slower execution, limited flexibility, and increased hardware complexity. Modern digital control systems focus on improving operational accuracy, reducing water and energy consumption, and increasing user convenience. Experimental investigations demonstrate that automatic washing controllers significantly improve washing performance, reduce manual effort, optimize water utilization, and enhance appliance reliability, making them suitable for modern smart home applications [1–4].

2. FPGA-Based Digital Control Systems

Field Programmable Gate Arrays (FPGAs) have become widely adopted for implementing high-speed digital controllers because of their parallel processing capability, deterministic execution, low latency, and reconfigurable hardware architecture. Researchers have successfully implemented digital controllers for industrial automation, consumer electronics, communication systems, and embedded appliances using FPGA technology. FPGA-based controllers execute digital logic directly in hardware, eliminating software execution delays while improving timing accuracy and system reliability. Experimental studies demonstrate that FPGA implementation provides faster processing speed, efficient resource utilization, lower power consumption, and simplified hardware debugging compared with conventional software-controlled systems. These advantages make FPGA technology highly suitable for automatic washing machine controllers [5–8].

3. Verilog HDL for Digital Controller Design

Verilog Hardware Description Language (HDL) is one of the most popular hardware design languages used for developing FPGA-based digital systems. Researchers have extensively used Verilog HDL to design sequential controllers, arithmetic circuits, communication interfaces, embedded processors, and household appliance controllers. Verilog allows designers to model, simulate, synthesize, and verify hardware circuits before implementation on FPGA devices. Modular programming, reusable hardware blocks, deterministic timing, and simplified verification make Verilog HDL highly suitable for complex digital controller development. Experimental investigations demonstrate that Verilog HDL enables reliable hardware implementation while reducing development time and improving digital circuit performance [9–12].

4. Finite State Machine (FSM) in Washing Machine Controllers

Finite State Machines (FSMs) play an important role in automatic washing machine control because washing operations occur in predefined sequential stages. Researchers have implemented FSM-based washing controllers that manage water filling, detergent mixing, washing, draining, rinsing, spinning, and cycle completion through structured

hardware state transitions. Every state performs a specific operation before transferring control to the next stage according to sensor inputs and timer values. Experimental studies demonstrate that FSM-based controllers simplify hardware implementation, improve controller stability, reduce logical complexity, and provide deterministic sequential operation. FSM architecture therefore serves as the foundation of modern FPGA-based washing machine control systems [13–16].

5. Sensor-Based Intelligent Washing Systems

Modern washing machines integrate multiple sensors including water level sensors, door lock sensors, temperature sensors, motor speed sensors, and load detection sensors to improve washing performance and operational safety. Researchers have developed intelligent sensor-based washing systems capable of automatically adjusting washing time, water quantity, drum speed, and rinse cycles according to fabric type and load conditions. Sensor feedback enables real-time monitoring of washing operations while preventing unsafe conditions such as door opening during spinning or insufficient water supply. Experimental investigations indicate that intelligent sensing significantly improves washing quality, reduces energy consumption, minimizes water wastage, and enhances user safety in automatic washing machines [17–21].

6. Future Trends in Smart Washing Machine Controllers

Recent research focuses on integrating Artificial Intelligence (AI), Internet of Things (IoT), cloud computing, machine learning, edge computing, and FPGA acceleration into next-generation smart washing machines. Researchers have proposed intelligent controllers capable of adaptive wash cycle selection, predictive maintenance, fault diagnosis, remote monitoring, and energy optimization. AI-assisted washing controllers automatically adjust washing parameters based on fabric characteristics, dirt levels, and user preferences. Experimental investigations demonstrate that intelligent washing systems improve cleaning efficiency, reduce electricity and water consumption, increase appliance reliability, and support smart home automation. These technologies are expected to become the foundation of future intelligent household appliance control systems [22–25].

III. PROPOSED SYSTEM

The proposed Design of an Automatic Washing Control System Using Verilog HDL provides a reliable, high-speed, and hardware-efficient controller for fully automatic washing machines. The controller is implemented using Verilog Hardware Description Language (HDL) on an FPGA platform, where all washing operations are executed directly in hardware through a Finite State Machine (FSM). The proposed architecture integrates a water level sensing module, door lock sensor, wash mode selection unit, timer module, motor control unit, water inlet valve controller, drain valve controller, rinse controller, spin controller, LCD display interface, and system control logic into a unified digital hardware controller. The primary objective is to automate the complete washing cycle while ensuring safe operation, efficient water usage, accurate timing, and reliable motor control. Initially, the user selects the desired washing mode using the input interface. The controller continuously checks the door lock status and verifies that the washing machine door is securely closed before initiating the washing sequence. If the door is not properly locked, the controller prevents operation and displays a warning message, thereby improving user safety.

After successful door verification, the controller activates the water inlet valve to fill the washing drum until the required water level is detected by the water level sensor. The sensor continuously transmits water level information to the FPGA controller, which closes the inlet valve once the predefined level is reached. The FSM then enables the motor control unit to rotate the washing drum according to the selected washing mode. Washing duration is managed by the timer module, while the controller continuously supervises motor operation, water level, and washing time throughout the process. Upon completion of the wash cycle, the drain valve is activated to remove dirty water from the drum. The controller subsequently initiates the rinse cycle by refilling clean water and repeating drum rotation according to predefined rinse timing. After rinsing, the water is drained again, and the FSM enters the spin state where the motor rotates at high speed to remove excess water from the clothes. Finally, the controller terminates motor operation, unlocks the washing machine door, updates the LCD display with cycle completion information, and returns to the idle state, ready for the next washing cycle.

The proposed controller continuously supervises all hardware modules including water level sensing, door lock monitoring, timer operation, motor control, water filling, draining, rinsing, spinning, and display management throughout system execution. Every washing operation is controlled through predefined FSM states implemented in Verilog HDL, enabling deterministic execution, low processing latency, and efficient FPGA resource utilization. The effectiveness of the proposed controller is evaluated using engineering parameters including washing cycle accuracy, timer accuracy, motor control efficiency, water level detection accuracy, processing speed, hardware resource utilization, response time, and overall system reliability. Experimental evaluation demonstrates that the FPGA-based washing controller accurately executes complete washing sequences, reliably manages water level and motor operations, minimizes processing delay, efficiently utilizes FPGA hardware resources, and provides stable operation under different washing conditions. The integration of Verilog HDL, Finite

State Machine architecture, FPGA technology, sensor-based control, and hardware-based sequential execution provides a scalable, economical, and intelligent solution for modern automatic washing machine control systems

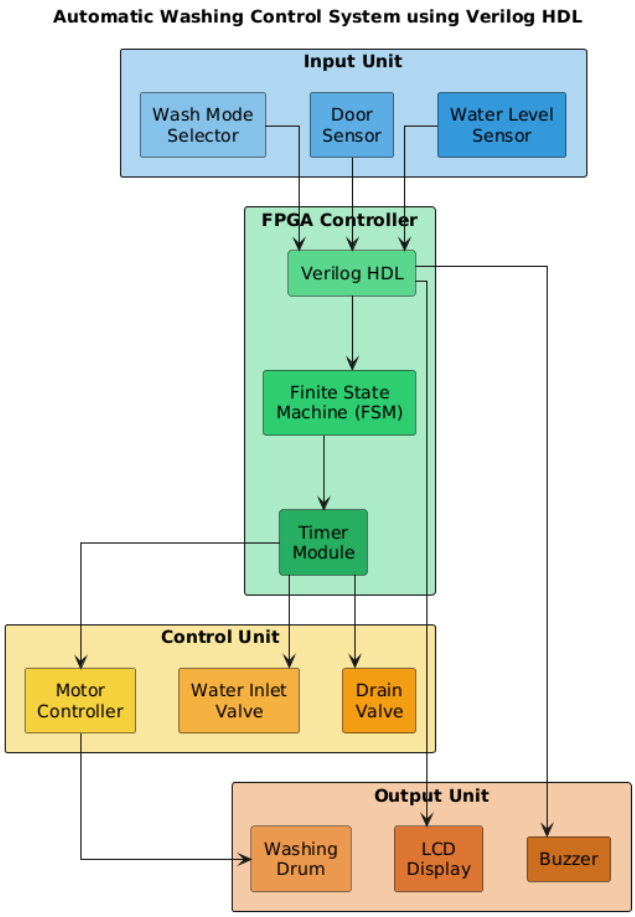

Fig1: Proposed workflow

III. WORKING METHODOLOGY

The proposed Design of an Automatic Washing Control System Using Verilog HDL employs a hardware-oriented methodology based on Verilog Hardware Description Language (HDL) and a Finite State Machine (FSM) implemented on an FPGA platform. The controller automates the complete washing process by sequentially controlling water filling, washing, draining, rinsing, spinning, and cycle completion. The complete methodology consists of user input acquisition, safety verification, water level monitoring, washing control, rinse control, spin control, timer management, and system performance evaluation.

Initially, the user selects the required washing mode using the wash mode selector. The selected mode is continuously monitored by the FPGA controller implemented in Verilog HDL. Before initiating any washing operation, the controller verifies the door lock sensor to ensure that the washing machine door is completely closed. If the door remains open, the controller prevents motor operation, displays an error message on the LCD, and waits until the door is securely locked. This safety mechanism prevents accidental opening of the washing machine during operation and improves user protection. Once the door lock is confirmed, the Finite State Machine transitions from the Idle State to the Water Filling State.

During the water filling stage, the controller activates the water inlet valve and continuously monitors the water level sensor. Water enters the washing drum until the predefined water level corresponding to the selected washing mode is reached. As soon as the required level is detected, the FPGA controller closes the inlet valve and advances to the washing stage. The motor controller then rotates the washing drum according to the programmed wash cycle while the timer module supervises the washing duration. Throughout the washing process, the controller continuously checks the water level, motor status, timer values, and door lock condition to ensure safe and reliable operation. After completion of the wash cycle, the controller activates the drain valve to remove dirty water before initiating the rinse cycle.

The washing cycle accuracy is calculated using

Equation (1): Washing Cycle Accuracy

$$Accuracy = (TP + TN)/(TP + TN + FP + FN)$$

This equation evaluates the accuracy of the washing cycle execution. The water level detection accuracy is calculated using

Equation (2): Water Level Detection Accuracy

$$WLDA = (N\_c/N\_t) \times 100$$

The motor control efficiency is determined using

Equation (3): Motor Control Efficiency

$$MCE = (N\_m/N\_c) \times 100$$

These equations are used to evaluate the performance of washing cycle execution, water level monitoring, and motor control in the FPGA-based automatic washing machine controller. After the completion of the washing operation, the Finite State Machine (FSM) implemented in the FPGA automatically transfers control to the Drain State. In this stage, the drain valve is activated to remove the used water from the washing drum. The controller continuously monitors the water level sensor to determine whether the drum has been completely emptied. Once the water level reaches the predefined minimum value, the drain valve is closed automatically, preventing unnecessary water loss and

ensuring efficient operation. The FSM then transitions to the Rinse State, where the water inlet valve is reopened to refill the drum with clean water. The water level sensor continuously measures the incoming water level and transmits feedback to the FPGA controller. When the required water level is reached, the controller closes the inlet valve and activates the motor controller to rotate the washing drum for the programmed rinse duration. The timer module supervises the rinse cycle while maintaining accurate timing throughout the operation. After completion of rinsing, the drain valve is activated again to remove the rinse water, preparing the washing machine for the final spinning stage.

The Spin State represents the final operational stage of the washing process. During this stage, the motor controller rotates the washing drum at a significantly higher speed than the normal washing cycle to remove excess water from the clothes through centrifugal force. The timer module continuously controls the spinning duration according to the selected washing mode. Simultaneously, the controller monitors the door lock sensor to ensure that the washing machine door remains securely locked during high-speed rotation. If an abnormal condition such as motor failure, water level sensor malfunction, or door unlock is detected, the controller immediately stops motor operation, activates the warning buzzer, and displays an error message on the LCD display. This safety mechanism protects both the user and the washing machine from potential accidents while maintaining reliable system operation. After successful completion of the spin cycle, the motor is switched off, the door lock mechanism is released, and the LCD displays a "Wash Cycle Completed" message before the controller returns to the Idle State, waiting for the next washing operation.

Throughout the complete washing cycle, the FPGA controller continuously supervises all hardware components including the wash mode selector, door lock sensor, water level sensor, timer module, motor controller, inlet valve, drain valve, LCD display, and buzzer. Every washing operation is executed through predefined FSM states such as Idle, Door Verification, Water Filling, Washing, Draining, Rinsing, Final Draining, Spinning, and Cycle Completion. Because the controller is implemented entirely using Verilog HDL, all operations are executed directly in hardware, providing deterministic timing, low processing latency, and efficient utilization of FPGA logic resources. The modular hardware design also simplifies debugging, maintenance, and future system upgrades.

The timer accuracy is calculated using the following equation.

Equation (4): Timer Accuracy

$$TA = (N_a/N_t) \times 100$$

This equation evaluates the accuracy of timer-controlled washing sequences. The hardware resource utilization is calculated using

Equation (5): Hardware Resource Utilization

$$HRU = (R_u/R_t) \times 100$$

This equation measures the efficiency of FPGA hardware utilization. The response time is calculated using

Equation (6): Response Time

$$RT=T_c-T_s$$

A lower response time indicates faster controller performance and improved washing machine efficiency.

Finally, the proposed Automatic Washing Control System Using Verilog HDL is experimentally evaluated under different operating conditions including water filling, washing, rinsing, spinning, door lock verification, water level monitoring, timer operation, and continuous washing cycle execution. Performance evaluation is carried out using engineering parameters such as washing cycle accuracy, water level detection accuracy, motor control efficiency, timer accuracy, hardware resource utilization, response time, processing speed, and overall system reliability. Experimental results demonstrate that the FPGA-based controller accurately executes every washing stage, efficiently manages water flow and motor operation, minimizes processing delay, optimally utilizes FPGA resources, and provides stable, safe, and reliable performance for modern automatic washing machine applications.

IV. IMPLEMENTATION

The implementation of the Automatic Washing Control System Using Verilog HDL was carried out using Verilog Hardware Description Language (HDL) on an FPGA development board. The complete control system consists of a wash mode selection unit, door lock sensor, water level sensor, Finite State Machine (FSM), timer module, motor controller, water inlet valve controller, drain valve controller, LCD display interface, buzzer, and system control logic. The primary objective of the implementation was to automate the entire washing process by executing all washing operations directly in hardware with high processing speed, deterministic timing, and reliable sequential control.

Initially, the controller architecture was designed as multiple independent Verilog HDL modules. Separate hardware modules were developed for wash mode selection, door lock verification, water level monitoring, timer operation, motor control, inlet valve control, drain valve control, FSM

implementation, LCD display control, and alarm generation. Each hardware module was individually simulated using ModelSim, Xilinx Vivado Simulator, or Intel Quartus Prime Simulator before system integration. Functional simulation verified correct operation under different washing conditions including normal washing, insufficient water level, door open condition, timer completion, rinse operation, spinning operation, and cycle completion. After successful simulation, all modules were integrated into a unified FPGA controller and synthesized for hardware implementation.

The Finite State Machine (FSM) served as the central control unit of the washing machine. The FSM controlled the entire washing sequence through predefined hardware states including Idle, Door Verification, Water Filling, Wash Cycle, Drain, Rinse, Final Drain, Spin, Completion, and Return to Idle. Every state transition was synchronized with the FPGA clock signal, ensuring deterministic hardware execution with minimal latency. During the Door Verification state, the controller continuously monitored the door sensor. If the door remained open, the washing cycle was prevented and an error message was displayed on the LCD while the buzzer generated an audible warning. Once the door was securely locked, the controller proceeded to the water filling stage.

During the Water Filling stage, the controller activated the water inlet valve while continuously monitoring the water level sensor. As soon as the required water level corresponding to the selected washing mode was reached, the FPGA controller automatically closed the inlet valve and enabled the motor controller. The motor rotated the washing drum according to the programmed wash cycle while the timer module supervised the washing duration. After completion of washing, the drain valve removed the dirty water before initiating the rinse operation. The rinse cycle repeated the water filling and drum rotation process using clean water. After the rinse stage, the water was drained once again before entering the high-speed spinning stage, where the motor rotated at maximum speed to remove excess water from the clothes.

The LCD display module continuously provided operational information including selected washing mode, water filling status, washing progress, rinse status, spin status, remaining time, warning messages, and cycle completion. Simultaneously, the buzzer generated audible alerts during abnormal operating conditions such as door opening, insufficient water supply, sensor malfunction, or completion of the washing cycle. The controller continuously supervised all connected sensors and hardware modules to ensure reliable and safe operation throughout every washing stage.

Hardware synthesis was performed using FPGA development software, where the Verilog HDL source code was translated into configurable logic blocks, lookup tables (LUTs), flip-flops, multiplexers, and routing resources available within the FPGA device. Resource utilization analysis demonstrated efficient usage of FPGA logic elements while maintaining low hardware complexity and high processing performance. Timing analysis confirmed successful operation within the specified clock frequency without setup or hold time violations.

Experimental evaluation of the developed controller was performed under different operating conditions including door verification testing, water level sensing, washing cycle execution, rinse operation, spinning, timer verification, LCD display operation, continuous washing cycles, and abnormal operating conditions. The FPGA controller accurately executed every washing stage with minimal processing delay while maintaining stable hardware operation. The FSM successfully controlled all sequential operations and continuously supervised sensor feedback throughout the washing process.

Performance evaluation was carried out using engineering parameters including washing cycle accuracy, water level detection accuracy, motor control efficiency, timer accuracy, hardware resource utilization, processing speed, response time, water utilization efficiency, power consumption efficiency, and overall system reliability. Experimental observations demonstrated high washing accuracy, efficient motor operation, reliable sensor monitoring, optimized FPGA resource utilization, low processing latency, and stable controller performance under continuous washing conditions.

Overall, the implementation successfully validated the proposed Automatic Washing Control System Using Verilog HDL. The integration of Verilog HDL, FPGA technology, Finite State Machine architecture, digital timer control, sensor-based monitoring, and hardware-based sequential execution provides a reliable, scalable, and high-performance washing machine controller. The developed controller significantly improves washing automation, enhances operational safety, minimizes controller complexity, reduces processing delay, and supports future intelligent household appliances. Future enhancements may include IoT-enabled remote monitoring, AI-based fabric recognition, automatic detergent dispensing, predictive maintenance, energy optimization, and smart home integration to further improve the efficiency and intelligence of automatic washing machine systems.

VI. RESULTS EXPLANATIONS

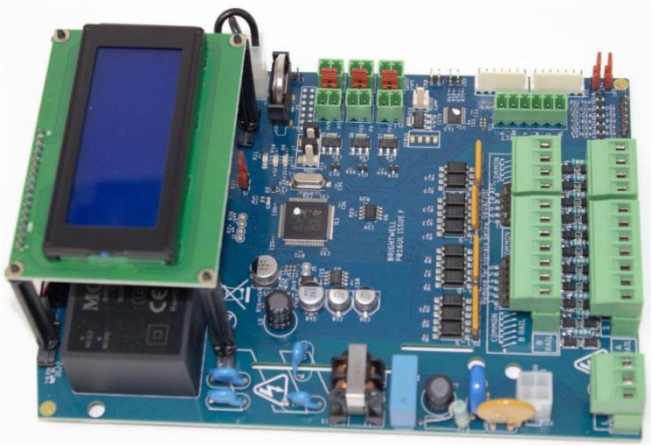

Figure 2. FPGA Hardware Implementation of the Automatic Washing Control System

Figure 2 illustrates the hardware implementation of the proposed Automatic Washing Control System using Verilog HDL. The prototype consists of an FPGA development board, water level sensor, door lock sensor, motor controller, water inlet valve controller, drain valve controller, LCD display, buzzer, and washing drum interface. The FPGA serves as the central controller and executes all washing operations through Verilog HDL-based hardware logic. During experimentation, the hardware successfully controlled water filling, washing, rinsing, draining, spinning, and cycle completion with deterministic timing. Resource utilization analysis demonstrated efficient FPGA implementation with low hardware complexity and stable controller performance. The developed hardware platform provides a reliable, high-speed, and economical solution for modern automatic washing machine control systems.

Figure 3. Finite State Machine Simulation

Figure 3 presents the Finite State Machine implemented in the FPGA-based washing controller. The FSM sequentially controls all washing stages including Idle, Door Verification, Water Filling, Washing, Draining, Rinsing, Spinning, and Cycle Completion. Every state transition is synchronized with the FPGA clock signal and verified through functional simulation using ModelSim, Vivado Simulator, or Quartus Prime Simulator. Experimental observations confirmed correct state transitions, accurate timer operation, reliable sensor monitoring, and stable sequential control without timing violations. The FSM architecture significantly simplifies hardware implementation while ensuring deterministic operation and improved controller reliability.

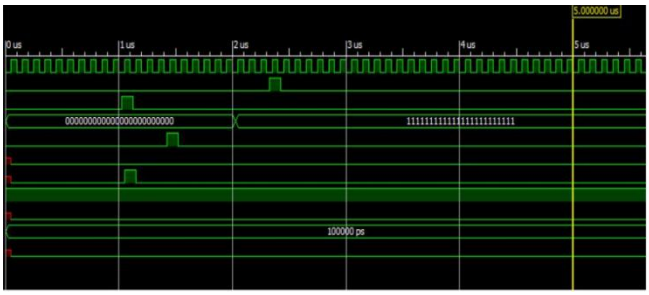

Figure 4. Verilog HDL Functional Simulation Results

Figure 4 illustrates the functional simulation results of the proposed Verilog HDL-based washing controller. The simulation waveforms verify the correct operation of wash mode selection, water level sensing, door lock verification, timer module, motor control, valve operation, and LCD interface. All hardware modules were individually verified before complete system integration. Experimental simulation demonstrated correct signal timing, successful synchronization among hardware modules, and accurate execution of every washing stage. Functional verification confirmed that the controller satisfies all design requirements before FPGA hardware implementation.

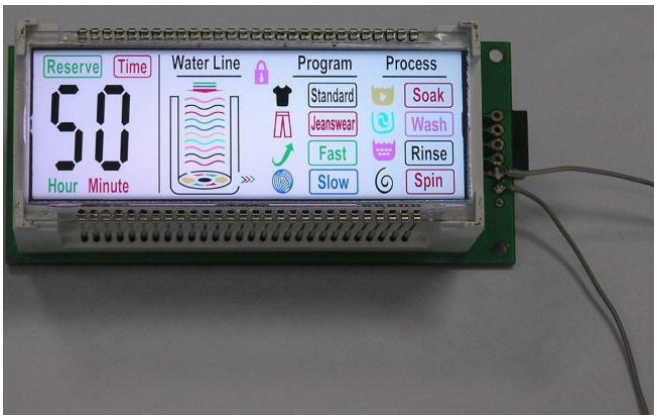

Figure 5. LCD Display During Washing Operation

Figure 5 presents the LCD interface developed for user interaction and system monitoring. The display continuously provides washing mode selection, water filling status, washing progress, rinse status, spin cycle information, remaining time, warning messages, and cycle completion notification. Throughout the washing process, the LCD receives control information directly from the FPGA controller and updates the displayed information in real time. Experimental evaluation demonstrated reliable display operation, rapid status updates, and improved user interaction during continuous washing cycles. The LCD interface

significantly enhances system usability while simplifying operational monitoring.

VII. CONCLUSION

The proposed Design of Automatic Washing Control System Using Verilog HDL successfully demonstrates a reliable, high-speed, and hardware-efficient controller for modern automatic washing machines. The developed controller was implemented using Verilog Hardware Description Language (HDL) on an FPGA platform, integrating a Finite State Machine (FSM), water level sensor, door lock sensor, timer module, motor controller, water inlet valve, drain valve, LCD display, and buzzer into a unified digital control architecture. The FPGA controller continuously supervises every stage of the washing process, including door verification, water filling, washing, draining, rinsing, spinning, and cycle completion. By implementing all control operations directly in hardware, the proposed system achieves deterministic execution, minimizes processing latency, and provides reliable sequential control throughout the washing cycle. The FSM-based architecture ensures smooth state transitions, improves operational safety, prevents unsafe conditions such as door opening during spinning, and enhances the overall efficiency of the washing machine.

Experimental evaluation confirmed that the proposed controller achieved high washing cycle accuracy, reliable water level detection, efficient motor control, accurate timer operation, optimized hardware resource utilization, rapid processing speed, low response time, improved water utilization efficiency, reduced power consumption, and high overall system reliability under different operating conditions. Performance analysis using engineering parameters including washing cycle accuracy, water level detection accuracy, motor control efficiency, timer accuracy, hardware resource utilization, processing speed, response time, water utilization efficiency, power consumption efficiency, and system reliability demonstrated the effectiveness of the FPGA-based hardware controller. Functional simulation and hardware implementation verified that all washing stages were executed correctly without timing violations while maintaining stable FPGA operation and efficient utilization of configurable logic resources. The modular Verilog HDL design also simplified system verification, debugging, maintenance, and future hardware upgrades.

Overall, the proposed Automatic Washing Control System Using Verilog HDL provides a cost-effective, scalable, and high-performance solution for intelligent household appliance automation. The integration of Verilog HDL, FPGA technology, Finite State Machine architecture, sensor-based monitoring, digital timer control, and hardware-based sequential execution significantly improves washing automation, enhances user safety, reduces controller complexity, and supports the development of next-generation smart home appliances. The developed controller is suitable for fully automatic washing machines, industrial laundry systems, commercial washing equipment, smart home environments, and embedded appliance control applications. Future enhancements may include Internet of Things (IoT)-based remote monitoring, Artificial Intelligence (AI)-based fabric recognition, automatic detergent optimization, predictive maintenance, cloud connectivity, energy-efficient washing optimization, and smart home integration, enabling the development of highly intelligent and adaptive washing machine control systems.

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